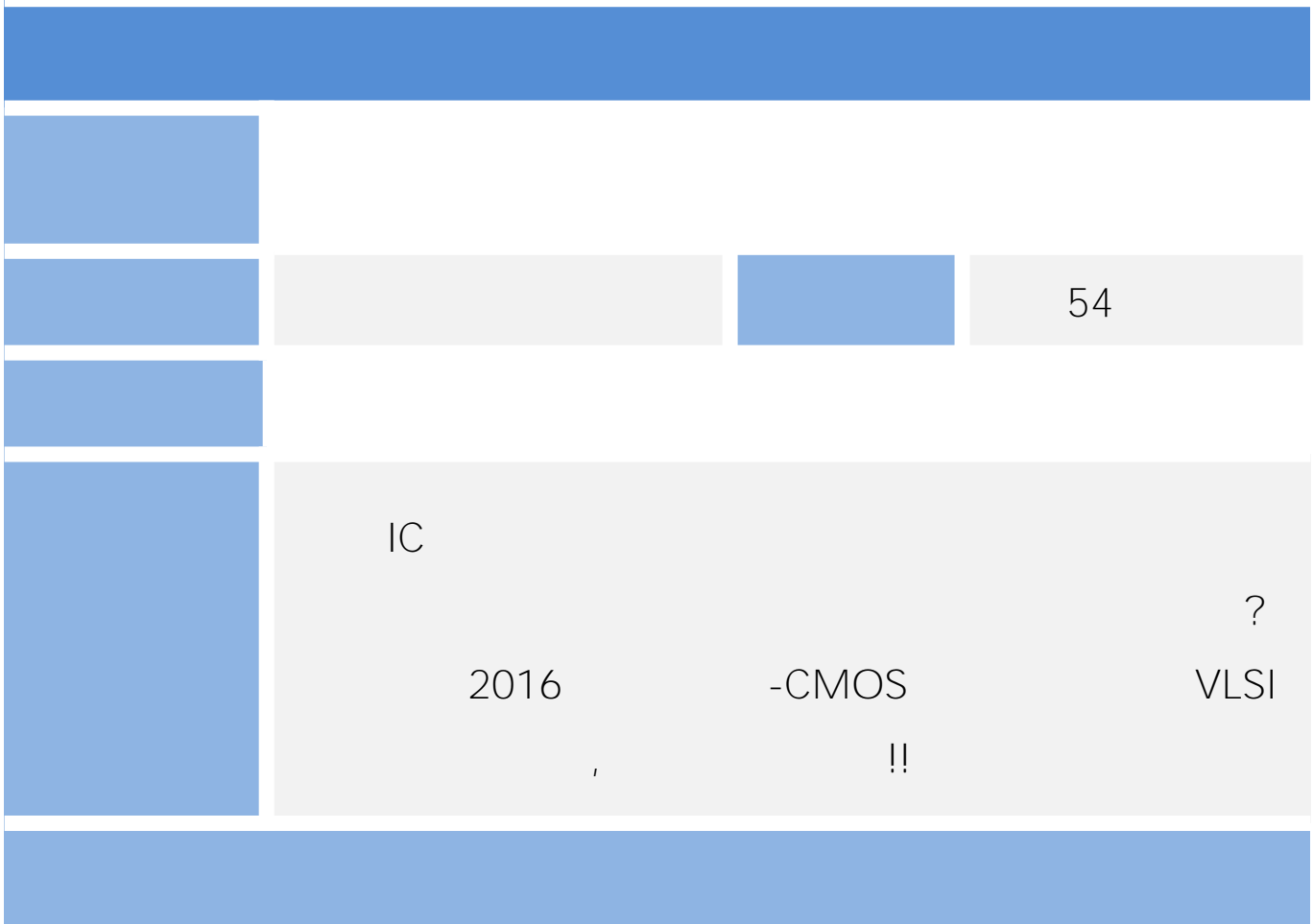


1. EDA
- 2.
3. FPGA
- 4.
- 5.
- 6.
- 7.
- 8.
9. ()
10. ()

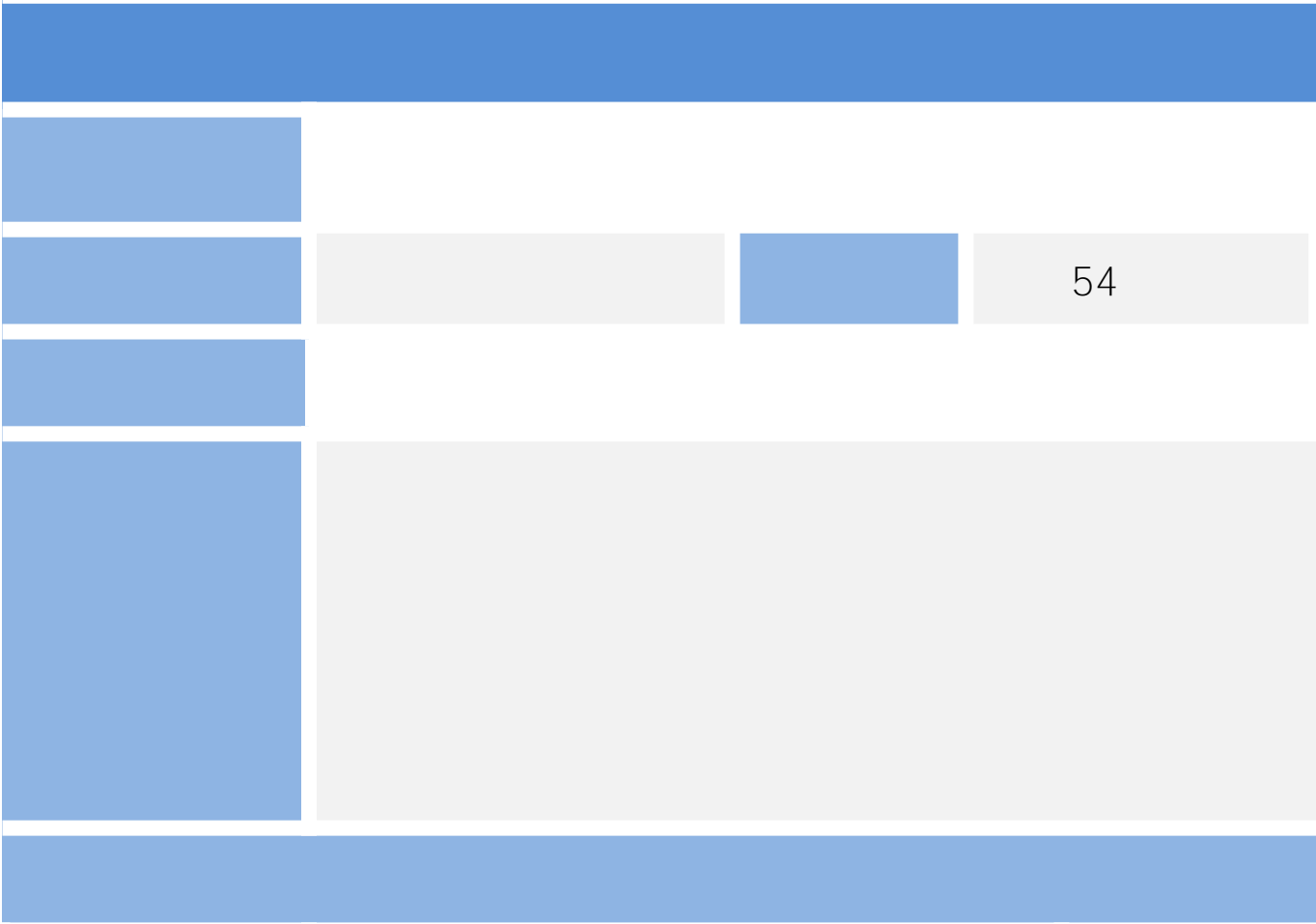


- SPICE
- 1. SPICE DC
- 2. MOS
- 3. .MEAS
- 4.
- 5. CMOS (1)
- 6. CMOS (2)
- 7. CMOS

33

- SPICE
- 1.
- 2.

21



(1)

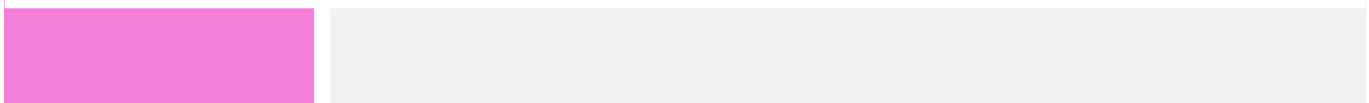
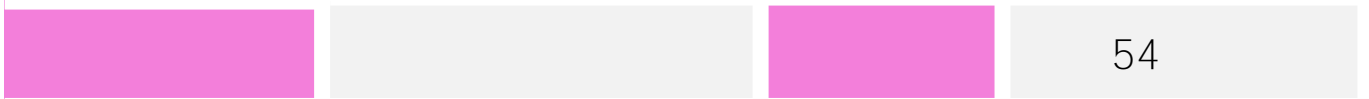
1. ()
2. OPA
- 3.

30

(2)

1. TI MSP430F149
2. IAR
3. GPIO
4. LCD module
5. LCD module
6. ADC 12
- 7.

24



1.					
2.Excel	()				
3.Excel	()		QQ		

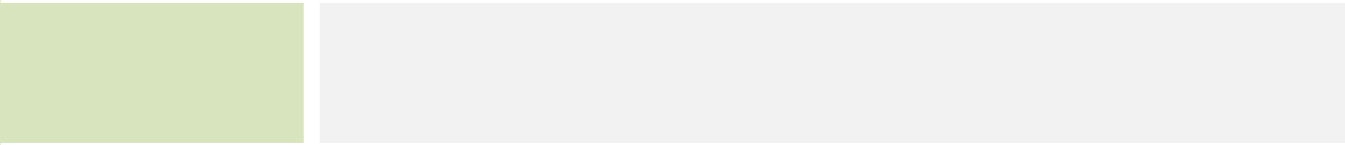
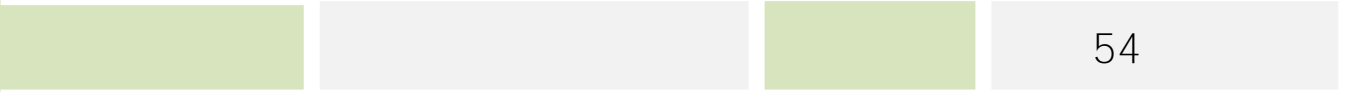
18

1.					
2.					
3.					
4.					
5.					

18

1.					
2.					
3.					
4.					

18



1. ()

2. (:)

3. (IDEO) + KJ

4.

5.

6.

18

1. 4.

2. 5.

3. 6.

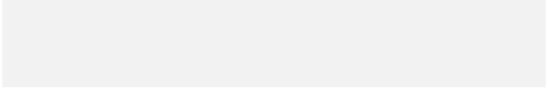
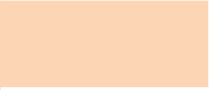
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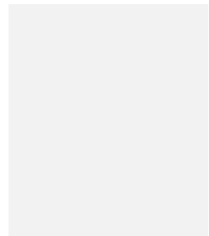
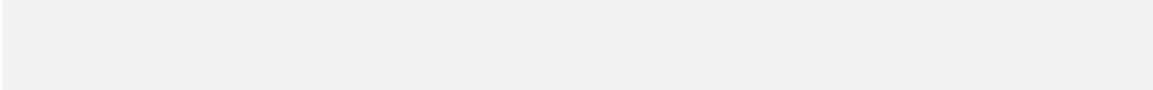
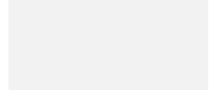
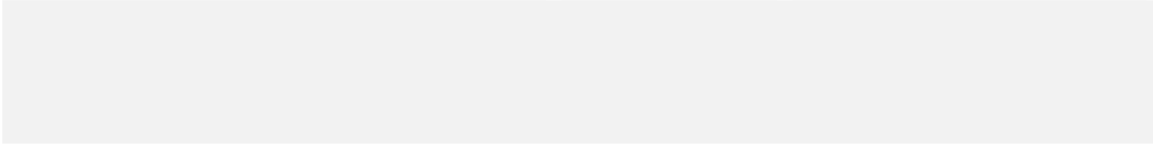
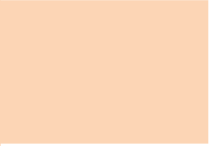
2. 5.

3. 6.

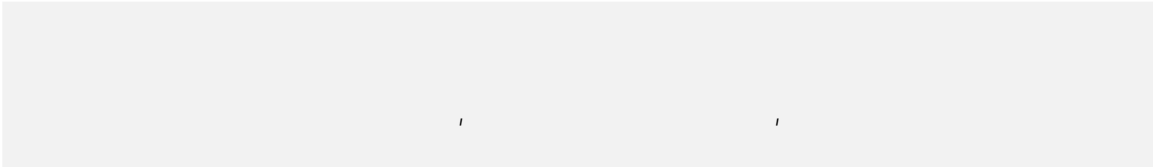
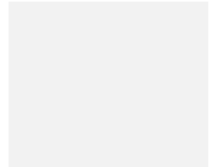
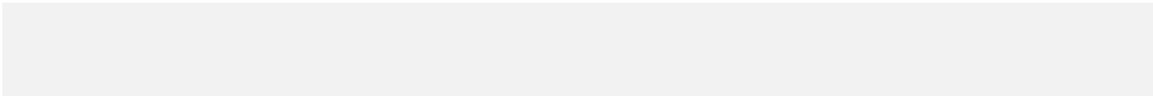
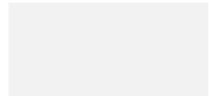
18



54



Design thinking
persona



-

prototype

Orange header bar

Orange block

Orange block

Grey block

Orange block

Grey block with number 54

Orange block

Large grey block

Wide orange bar

Grey block

Grey block

Grey block

Grey block

Orange block

Orange block

Grey block

Grey block

Grey block

Grey block

Orange block

Orange block

Grey block

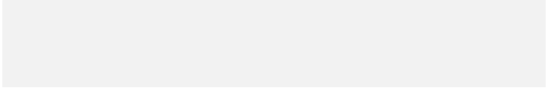
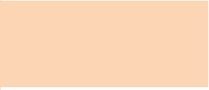
Grey block

Grey block

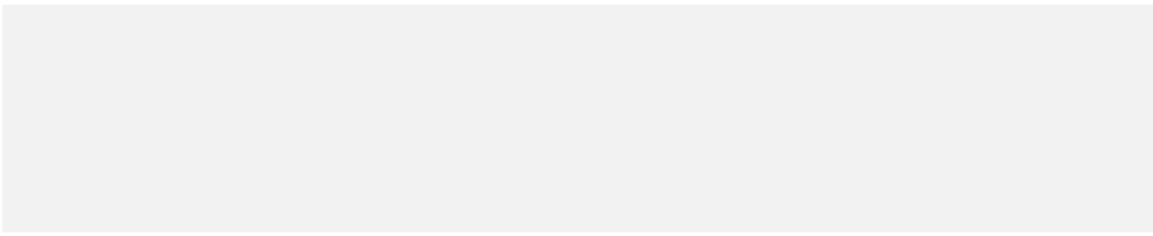
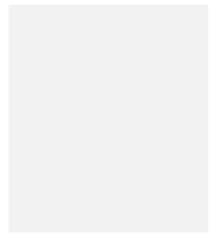
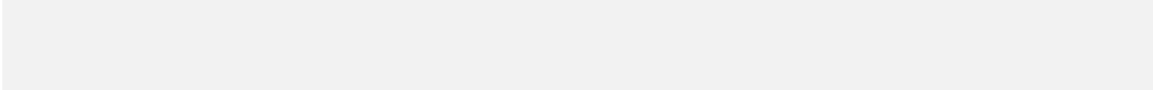
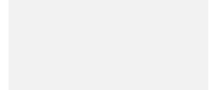
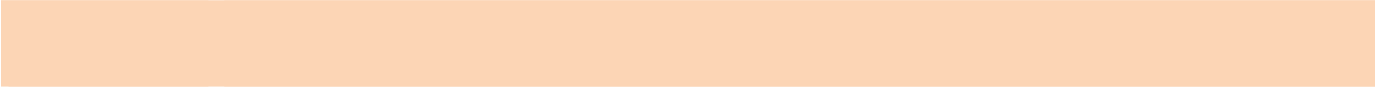
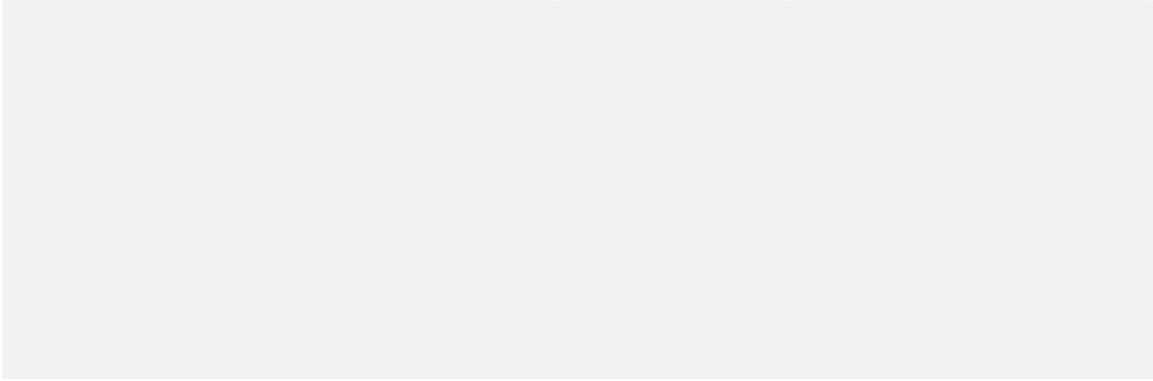
Grey block

Orange block

Orange block



54



BV

